STUDY ON REVERSIBLE LOGIC CIRCUITS AND ANALYSIS

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Abstract- Low power is the main agenda in analog and digital VLSI circuits design, in today's digital world. This study focuses on low power circuits using reversible logic gates. Reducing the number of constant inputs and minimizing the garbage outputs, in existing design is the objective. New Universal Reversible Logic gates Twin SJ and SMJ have been designed. Another gate by name DINV gate is also designed. Their inputs are suitably configured so that they perform various logic functions. Using these gates and other reversible logic gates, combinational circuit and sequential circuits are developed. Reversible D Flip Flop, Reversible T Flip Flop, and Reversible 5:32 decoder and Reversible 8:1 multiplexer circuit are developed. All circuits are coded on Xilinx tool using VHDL coding, simulated and verified.

Keywords: constant inputs, garbage outputs, Reversible logic combinational circuits, Reversible logic sequential circuits

I. INTRODUCTION

Reducing power is a magic word that has gained importance with development of deep sub micron and nanotechnologies. Low power consumption, which is requirement of the modern world as more PDAs - Personal Digital Assistant and other gadgets are being used by everyone irrespective of the age or area of business or study. There are many techniques for Low Power design. The "reversible logic design" attracts more interest. In this logic reduction in energy dissipation is achieved without destroying the information bits. In 1961 Rolf Landauer [7] proved that traditional logic gates or binary logic gates dissipate a certain amount of energy during computation. This is caused by loss of each bit of information. [6] kTln2 joules is the loss for each bit of information. In this K is the Boltzmann's constant and T is the temperature of operation. Charles Henry Bennett [7] showed in 1973, that [6] in order to avoid KTln2 joules of energy dissipation in an irreversible circuit, reversible logic gates will be of use, since there is no information loss in reversible circuits. However, fan-out is not possible in reversible Logic, as one to many cannot be reversed. If we assume proper technology, a reversible logic circuit can realize the inverse operation simply by applying the gates in the reverse order. Synthesis is possible either from the outputs toward the inputs or from the inputs toward the outputs.

In this paper [2] decoder 2:4 is built using Feynman and Fredkin gates. Using this 3:8 decoder is built. [1] in this paper decoders up to 4:16 are built. This work on 4:16 DECODER using, BVF F2G and FRG Gates was an improvement on Decoder using only FRG Gates. [4] HL gate and Rgate are built to construct the decoder circuits. [8] decoders are built on xilinx.

[1] The authors gave possible research directions to optimize other combinational and sequential circuits and to improve on low power and quantum cost. [1] The authors also suggested, other modifications in this research work to reduce garbage output value and number of constant inputs/outputs and quantum cost using other reversible gates such as Modified Fredkin gate, DPG or DKG gates.

[5] In this paper power efficiency is discussed. Main disadvantage is high number of constant inputs is used. Hence it has scope on improvement. Improvement on following the basic rule for Reversible Gates, i.e number of inputs should equal the number of outputs is possible by optimizing the constant inputs and garbage outputs.

[9] [10] Sequential circuits – the authors Himanshu Thapliyal and M.B Srinivas, developed D Flip Flop using modified Fredkin Gate. RS Flip Flop, JK Flip Flop, T Flip Flop, Master slave JK Flip Flop are built. The authors had built D Flip Flop with 7 gates and number of garbage outputs are 8 which is very high.

II. REVERSIBLE GATES

All digital functions in conventional method are irreversible. At any point of time, previous computations cannot be recovered. Operations required in computation could be performed in a reversible manner, thus dissipating no heat. One of the conditions for any circuit to be reversible is that its input and output be uniquely retrievable from each other or mapped one to one. The other condition is if a device can actually run backwards then it is called physically reversible. Basic Reversible Gates are Feynman Gate 2 x 2, Double Feynman Gate 3 x 3, Toffoli Gate 3 x 3, Fredkin Gate. 3 x 3, Peres Gate 3 x 3, TSG gate 4 x 4, Sayem Gate 4 x 4, to name a few. There are 3 x 3 and 5 x 5 gates built for unique applications in this study. The same gates can be used for other applications also.

Reversible Logic has the following Rules,

- Number of outputs equal that of inputs. n x n
- Unique input to output pattern
- Garbage outputs to be minimized
- Gate count should be minimum
- Constant value for inputs [‘0’ or ‘1’] should be reduced
- Fan-out should be NIL
- Feedback / Loop back circuit is not allowed

III. PROPOSED STUDY

This study focuses on building (i) Reversible sequential circuits such as REV D Flip Flop and REV T Flip Flop and (ii)Combinational circuits such as 5:32 REV decoder using 4:16 REV decoder, 8:1 REV mux and REV 16 Bit Latch using D Flip Flop. This study involves VHDL coding for the reversible logic circuit and to analyze the power consumption and reduce garbage outputs. In this study, designing of new reversible gates, Universal gate (Twin SJ gate),D INV gate, and building different reversible logic circuits - Flip Flops, decoders, multiplexer and Latch circuits using new design gates and other basic reversible gates is carried out. These circuits are built, simulated and the results are analyzed using Xilinx 14.7

NEW REVERSIBLE GATES

(I) DINV Gate This DINV GATE is reversible gate with 3 x 3 configurations. The outputs are mostly of AND configuration. The Outputs are A'.B, A.B and A.C. This gate is used in Decoder circuits.

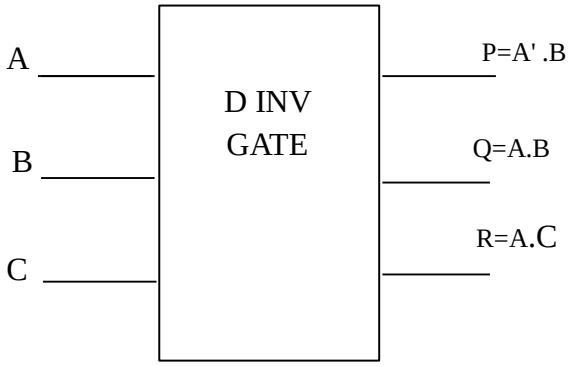

Figure 1 : DINV GATE

(II) TWIN SJ Gate This TWIN SJ GATE is reversible gate with 5 x 5 configuration with Outputs P=A'C+AD, Q=[(A+B).(C+D)]⊕E, R=B⊕E, S=A+E, T=B+E

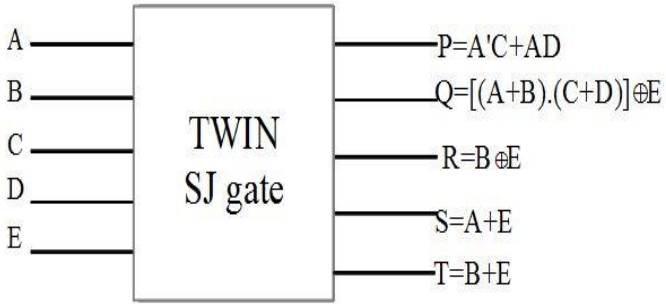

Figure 2 :TWIN SJ GATE

DINV gate and TWIN SJ gate are used in 4:16 and 5:32 DECODERS. Toffoli gate, Feynman Gate, Fredkin Gate, Peres gate and Dual AJ gate are common reversible gates used in Flip Flop, mux and Latch design.

REVERSIBLE D FLIPFLOP Flip flop is used for storage of data as it latches data. It stores the bit that is available at 'D' input. Change in D input is updated on rising edge of the next clock. I.e. a delay of one clock. Hence it is also Delay (D) flip Flop. Reversible D Flip Flop is built in VHDL coding. Also reversible gate FEYNMAN is used as a buffer or for duplicating the signals as fan out is not possible in Reversible Logic. D Flip Flop is simulated and verified in enabled and disabled conditions. Results are given in Figure 12

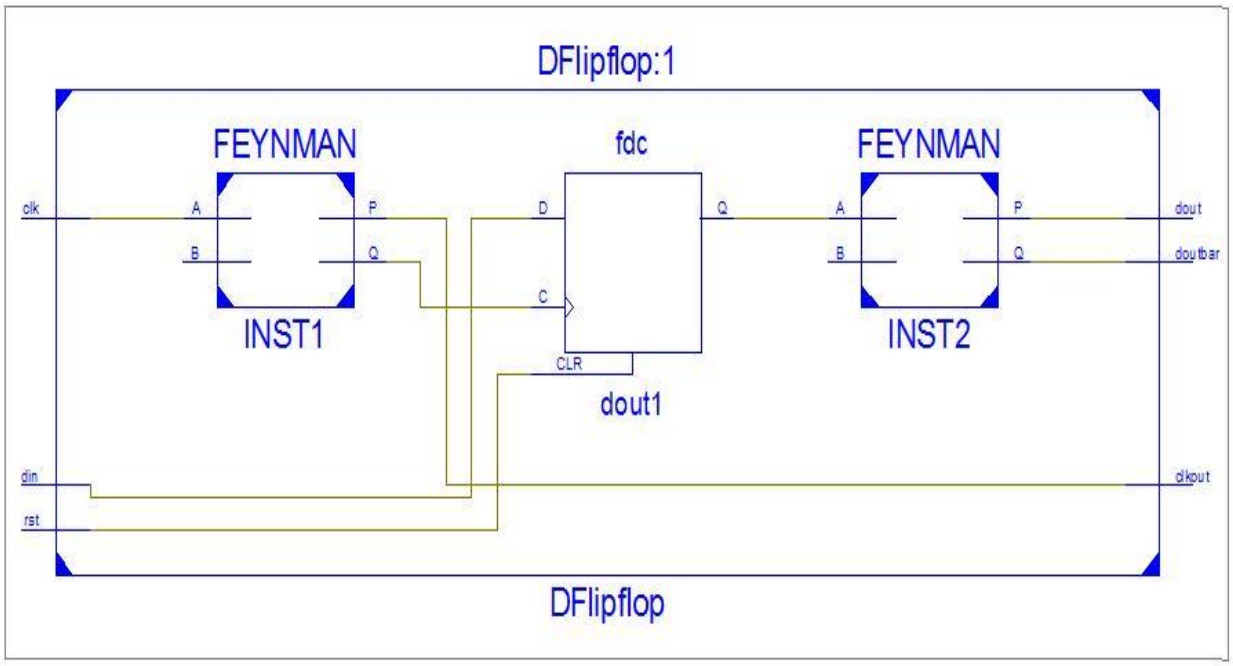

Figure 3: D FLIP FLOP RTL SCHEMATIC

REVERSIBLE T FLIPFLOP T Flip Flop changes its output on every clock i.e. it toggles. Hence the frequency of output is half of the input frequency. Output toggles on every rising edge of the clock. Reversible T Flip Flop is built in VHDL coding. Reversible gate FEYNMAN is used as a buffer or for duplicating the signals as fan out is not possible in Reversible Logic. T Flip Flop is simulated and verified in enabled and disabled condition. Results are given in Figure. 13

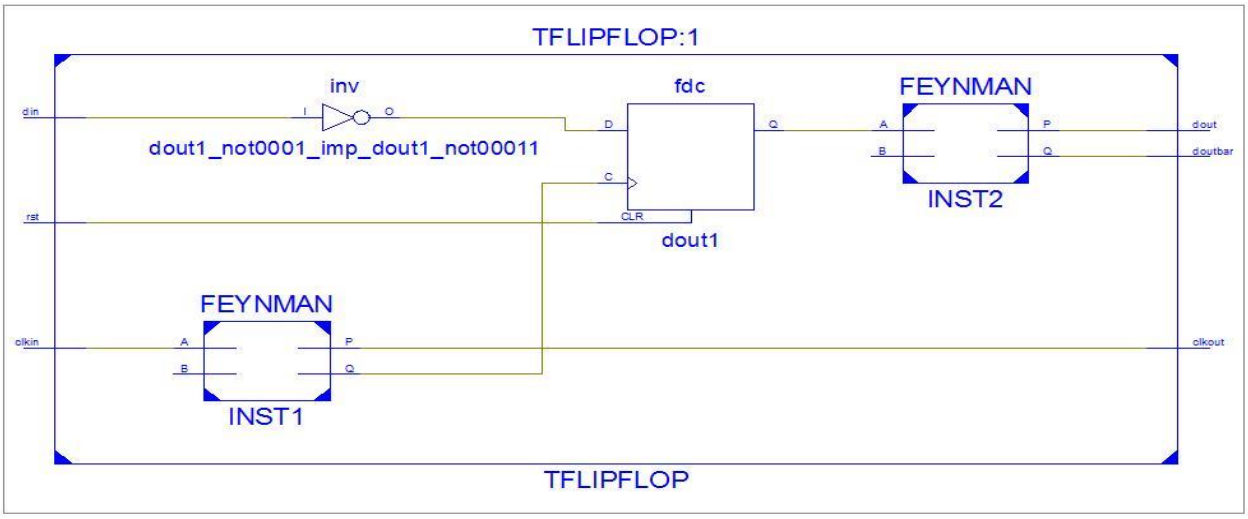

Figure 4: T FLIP FLOP RTL Schematic

REVERSIBLE 5: 32 DECODER

N:2^N Decoder is to select one out of 2^N output lines using suitable inputs. Decoders are normally used to select a particular device or memory location using suitable signal lines generally, Address lines. In this study, 5:32 Decoder is built using two 4:16 decoders and suitably enabling them with 5^{th} Input signal (I_4).

Block diagram Fig.5 and Fig.6, show the over all view of the Decoder. RTL schematic of 5:32 decoder with exploded view of 4:16 decoder is given Figure 7. Four numbers of Feynman gates are used for buffering the Input signals I_0 to I_3. I_0 to I_3 are connected to both 4:16 decoders. Enable signal 'EN' and I_4 are inputs to DINV gate. DINV is a new gate, used to select / enable either of the 4:16 decoders based on I_4. Outputs of DINV gate are enable signals for the 4:16 decoders. If I_4 is '0', then Decoder 1, for D0-D15 is enabled. If I_4 is '1', then Decoder 2, for D16 - D31 is enabled. Circuit developed for 5:32 Decoder is simulated and verified in enabled and disabled condition. Results are given in Figure. 14 and Figure 15. When 'EN' signal is '0', then all the bits are 'zero', for different states if I_0 to I_4. This is clearly visible in the results. 4:16 decoder is built with 3:8 decoder and Feynman Gates. 3:8 decoder is built with 2:4 decoder, DINV gate and Feynman Gates.

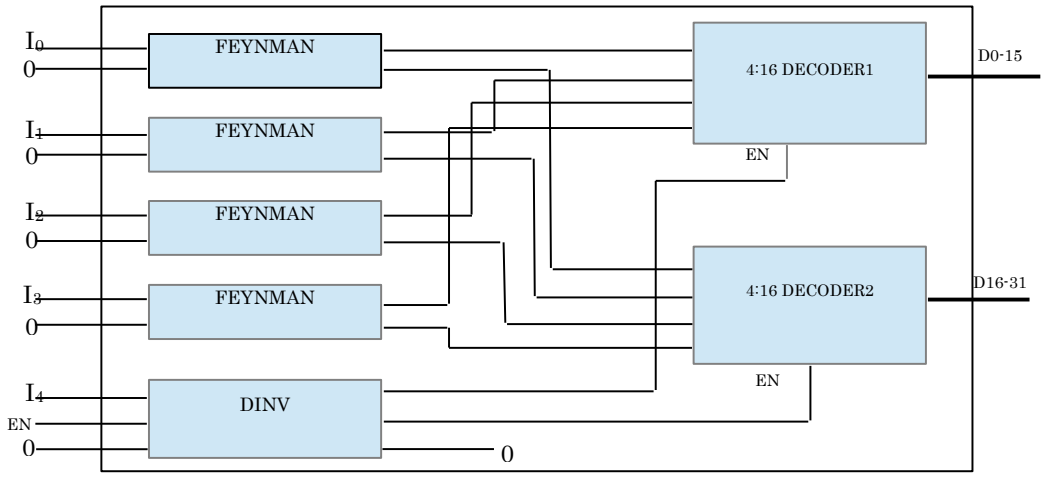

Figure 5 : 5:32 DECODER BLOCK DIAGRAM

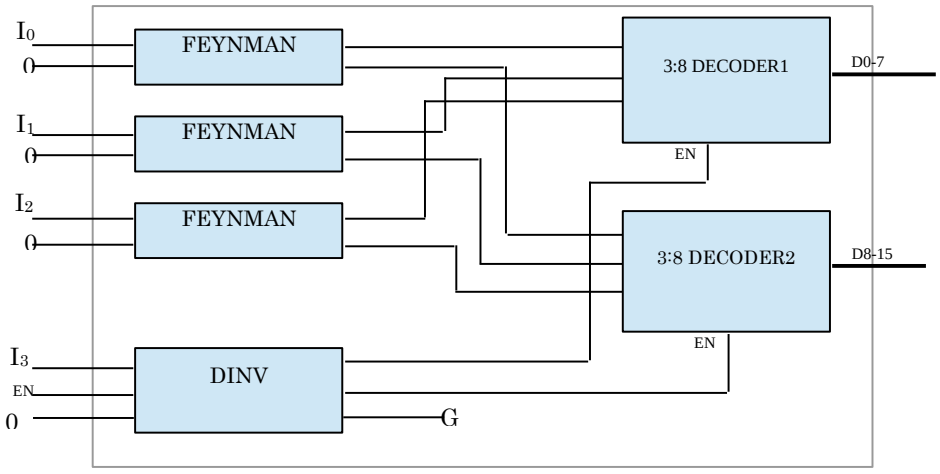

Figure 6: 4:16 DECODER

RTL Schematic of Decoder 5:32 with the exploded view of 4:16 decoders is given in Fig.7

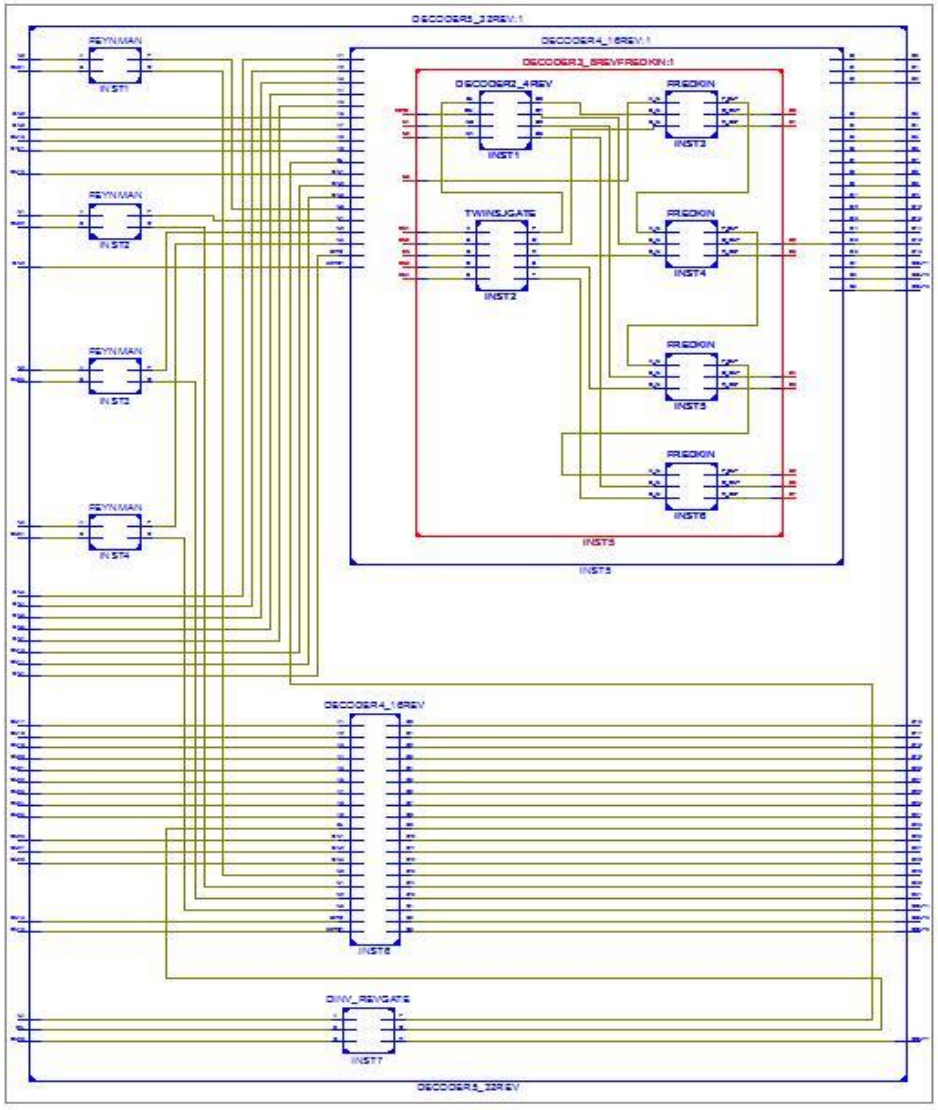

Figure 7: 5:32 DECODER RTL SCHEMATIC

REVERSIBLE MULTIPLEXER 8:1

Multiplexer is a combinational circuit used to connect one of the 2^n input lines witn 'n' select lines. In this study, one of the 8 inputs get connected to the output by three select lines. 8:1 Multiplexer has 3 select lines (SEL0 to SEL2) to choose one out of 8 inputs.

In reversible circuits, garbage outputs need to be optimized. Number of useful output is minimum in case of multiplexers. Two 4:1 multiplexers are used to build 8:1 multiplexer. 4: 1 multiplexers are built using 2:1 multiplexers and Feynman Gates. This circuit uses basic gates. No special gate is used. Reversible Feynman gate is a basic 2 x 2 gate. Outputs A and A XOR B (inputs A and B), enable to repeat or invert the signale based on input B. Giving '0' to B repeats A at both outputs.

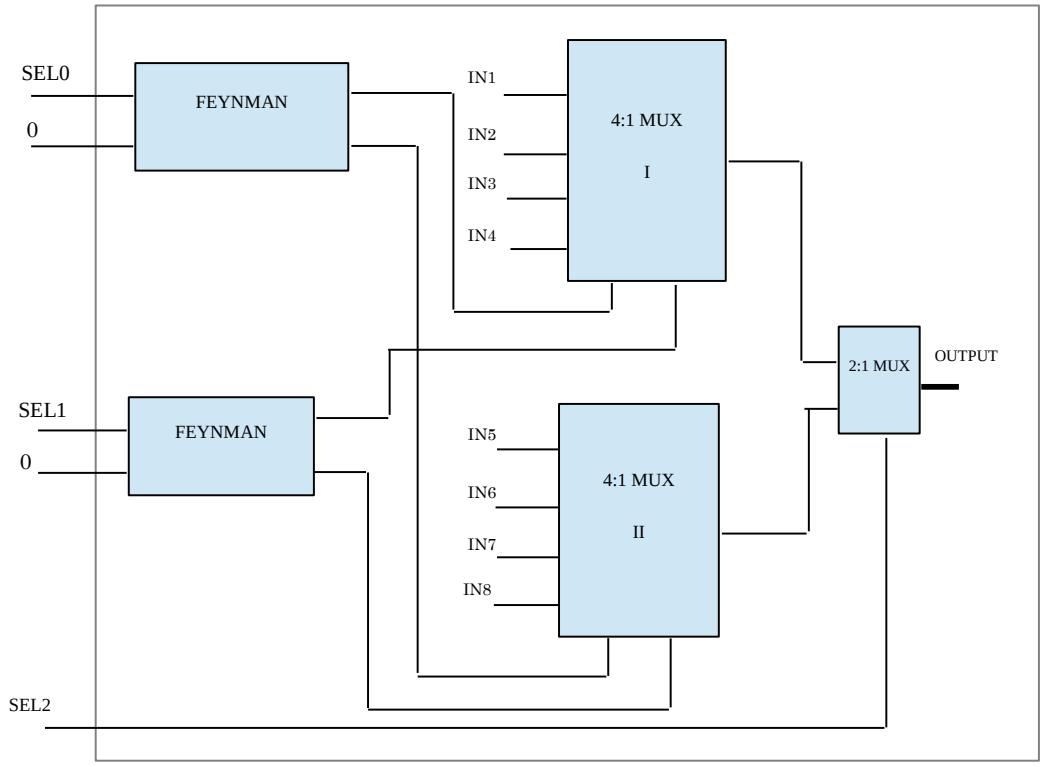

Figure 8: MULTIPLEXER 8:1 BLOCK DIAGRAM

Feynman gate is used to copy the select bits SEL0 and SEL1. Inputs v_in1 to v_in4 are connected to 4:1 mux I and Inputs v_in5 to v_in8 are connected to 4:1 mux II. Using selection bits SEL0 and SEL1, corresponding input is selected. Mux output from these 4:1 mux are connected to a 2:1 mux whose selection bit is SEL2.

For example, if the selection bits are 000, IN1 should be available at OUTPUT. IN1 is at the output of Mux I and IN5 is at the output of Mux II. These are inputs to 2:1 Mux. From these inputs, IN1 is selected by SEL2 (0) of the 2:1 Mux. As another example, if the selection bits are 101, IN6 should be available at OUTPUT. IN2 is at the output of Mux I and IN6 is at the output of Mux II. These are inputs to 2:1 Mux. From these inputs, IN6 is selected by SEL2 (1) of the 2:1 Mux. During simulation, To visualize the results, Inputs v_in1, v_in3, v_in5 and v_in7 are given '0' and v_in2, v_in4, v_in6 and v_in8 are given '1'. By giving combination of Selection bits with different timing, the output corresponding to the selection is shown at output. Ref. Fig 18 for the results of 8:1 Multiplexer

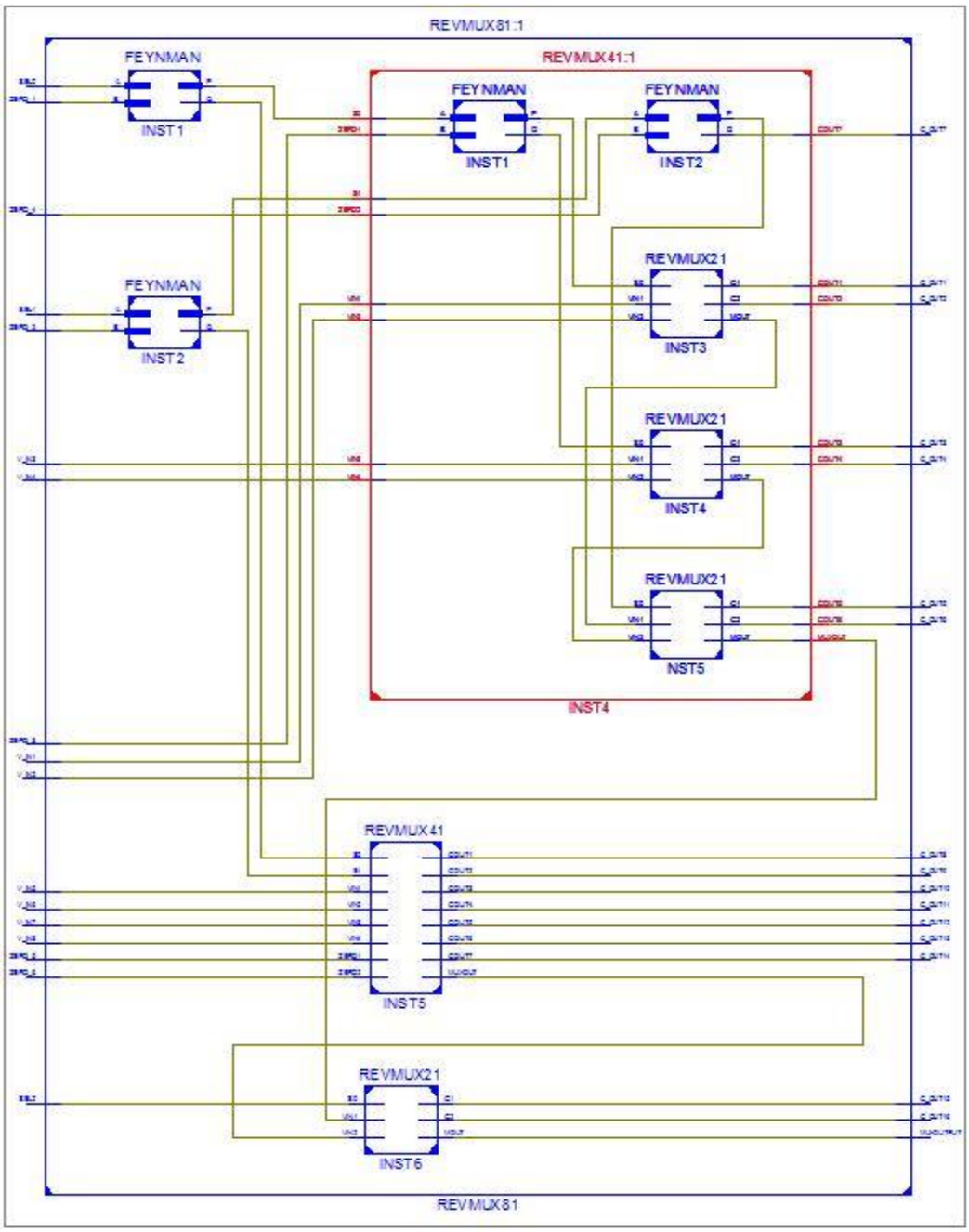

Figure 9: MULTIPLEXER 8:1 RTL SCHEMATIC

LATCH is a sequential logic circuit. 16 bit Latch circuit is used to hold data. D Flip Flop (latch) is used for storage of one bit. It gets updated on each clock. 16Bit latch has 16 D Flip Flops. Selection of Flip Flop is done using Decoder. By decoding the Address lines, particular memory bit can be accessed (Read / write). A block called 'Interface' is built using Feynman and Toffoli gates. RST of all D flip flops is connected from Interface Block. Input to Interface block, Toffoli gate is suitably given to set RST of particular D FlipFlop to '0'. Clock output (clkout) of one D flip flop is connected to the clock input of next D Flip Flop. This reduces the number of Garbage outputs. Din (D0 to D15) of D flip flops is the actual data to be stored. Data is updated at the rising edge of the input clock. Exploded view of Interface Block is given in Figure 10.

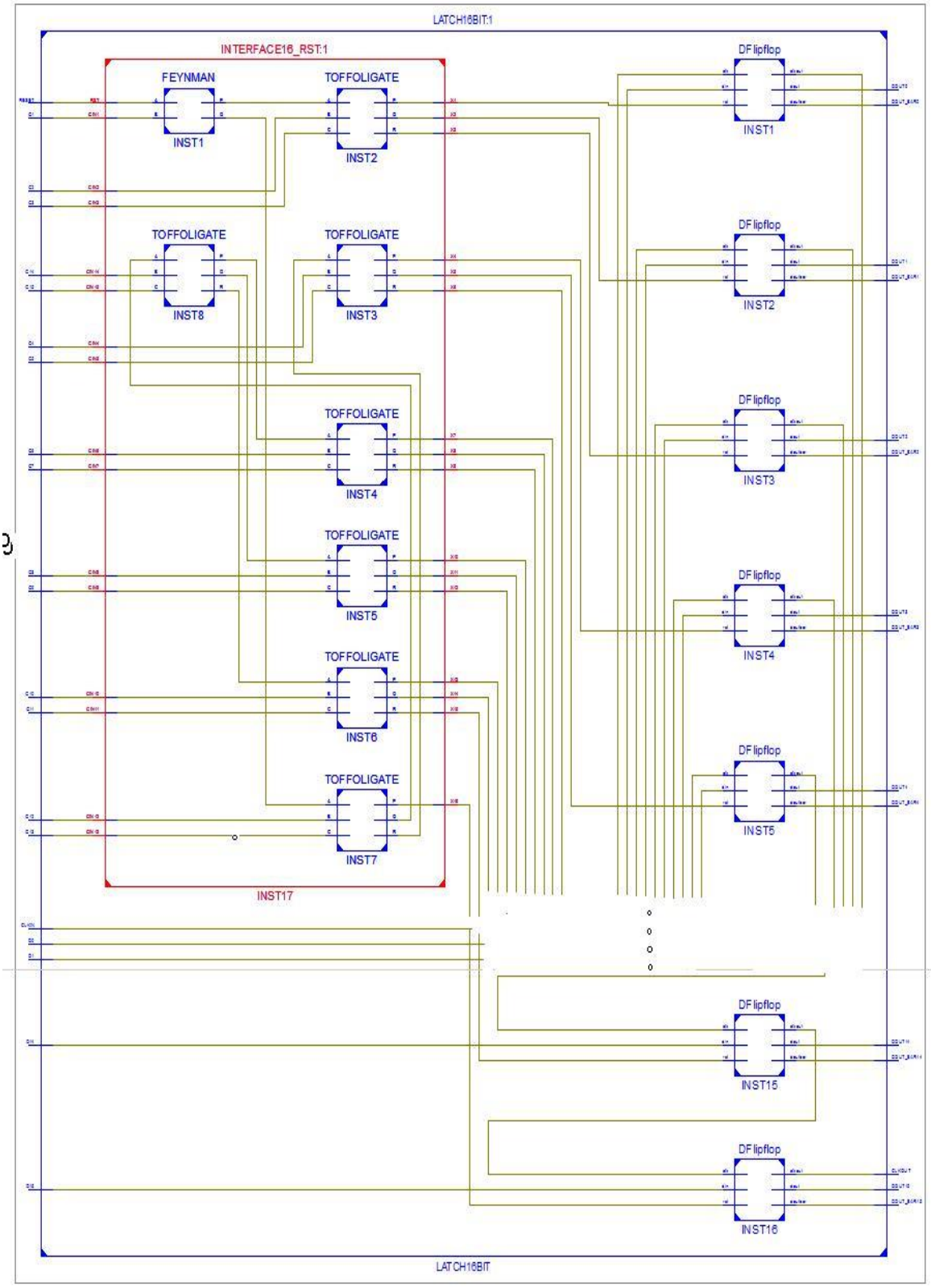

Figure 10: 16 BIT LATCH RTL SCHEMATIC (exploded view)

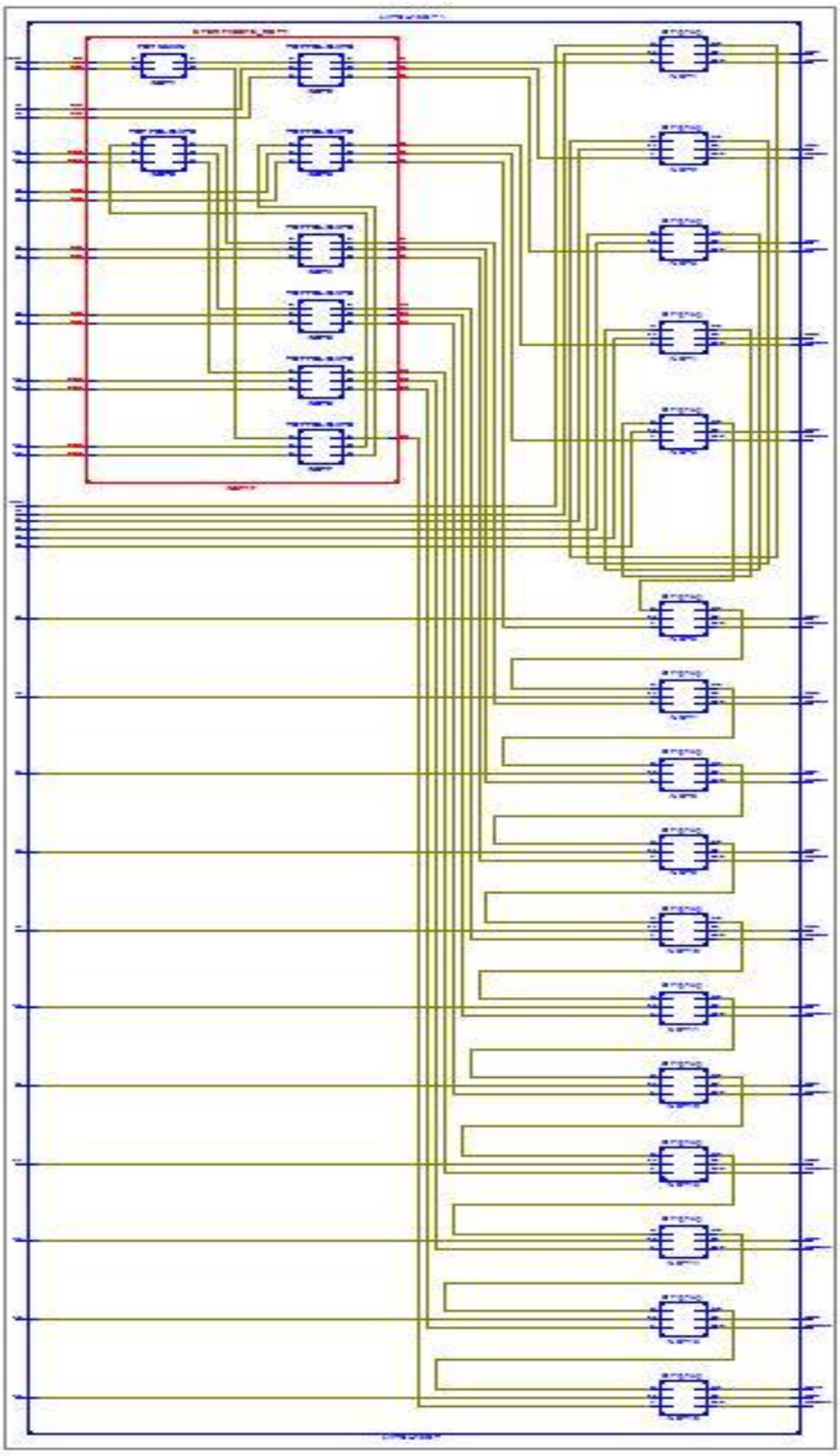

Figure 11: 16 BIT LATCH RTL SCHEMATIC

IV RESULT & CONCLUSION

Software Tool: In this study all the gates and circuits are built on Xilinx 14.7 tool. Xilinx ISE is a design environment software tool for synthesis and analysis of HDL designs. This enable us to synthesize (compile) the design and to

- perform timing analysis
- examine RTL diagrams
- analyse the responses for different stimuli

This tool has a limitation of not to be used with FPGA products of other manufacturers. Xilins ISE (circuit synthesis and design) + ISIM or modelsim logic simulator (used for system level testing).

D FLIPFLOP Initially reset (rst) is made to '1' and after a delay it is made to '0'. A rising pulse is given to reset, to clear. 20ns pulse is given as clock and 30ns pulse is given as data. The state change of data (din) is updated at the output (dout) during next rising edge of the clock (clk). In the given figure 12., at 0.60us, 'din' goes low and the 'clk' is low. Hence there is no change in 'dout'. At the next rising edge of the clock(0.62us), 'dout' goes low.

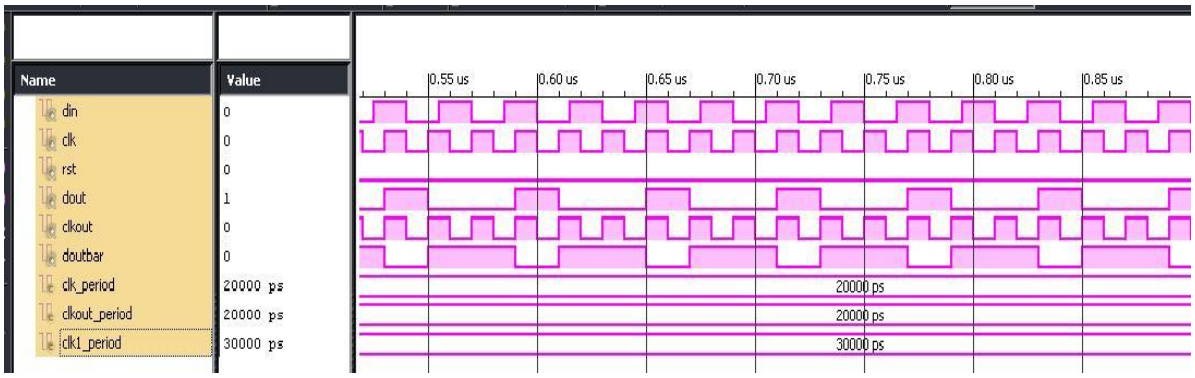

Figure 12: D FLIP FLOP RESULT

T FLIPFLOP Initially reset (rst) is made to '1' and after a delay it is made to '0'. A rising pulse is given to reset, to clear. 10ns pulse is given as clock. In the Figure 13., the output 'dout' changes state (toggles) when there is state change of data (din) during next rising edge of the clock (clk). In the given at 0.45us, 'din' goes low and the 'clk' is low. The 'dout' continues to be low. There is no change in 'dout'. At the next rising edge of the clock, at 0.455us, 'dout' goes High (toggled). At 0.6us 'din' goes high and the 'clk' is low. The 'dout' continues to be high. There is no change in 'dout'. At the next rising edge of the clock, at 0.655us 'dout' goes low (toggled).

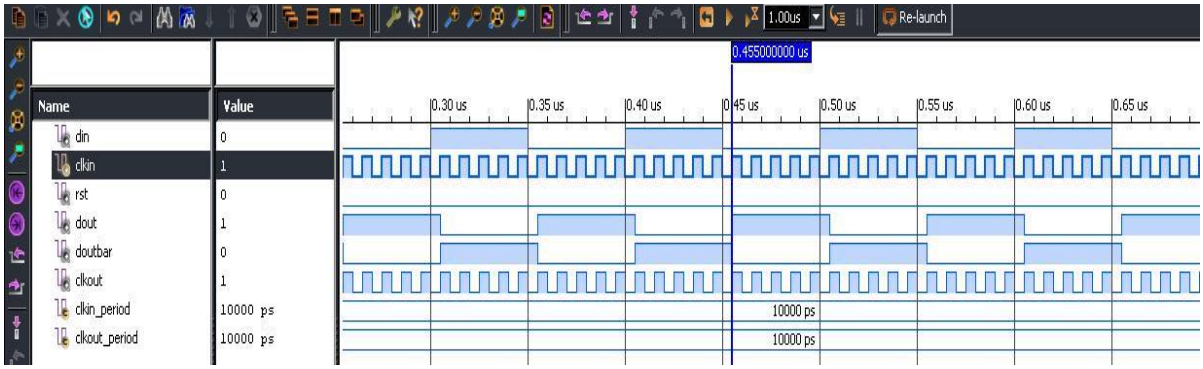

Figure 13: T FLIP FLOP RESULT

DECODER5:32 Results are given in Figure. 14 to Figure 17. When 'EN' signal is '0', then all the outbit bits d0 to d31 remain 'zero', for different states of I_0 to I_4. In Figure.14, at 0.81us in0 and in1 are '1' and in2, in3 and in4 are '0', '00011' corresponding bit 'd3' is selected. Similarly in Figure.15, at 2.39us, in3, in1 and in0 are '1', in2 and in4 are '0',01011 is the input and corresponding bit 'd11' is selected. In Figure.16, at 3.99us, in0, in1 and in4 are '1' and in2 and in3 are '0', '10011' corresponding bit 'd19' is selected. Similarly in Figure.17, at 5.6us, in4, in3, in1 and in0 are '1', in2 is '0', 11011 is the input and corresponding bit 'd27' is selected. It can be noted that when 'EN' is low, though the input signals were active, no output is available.

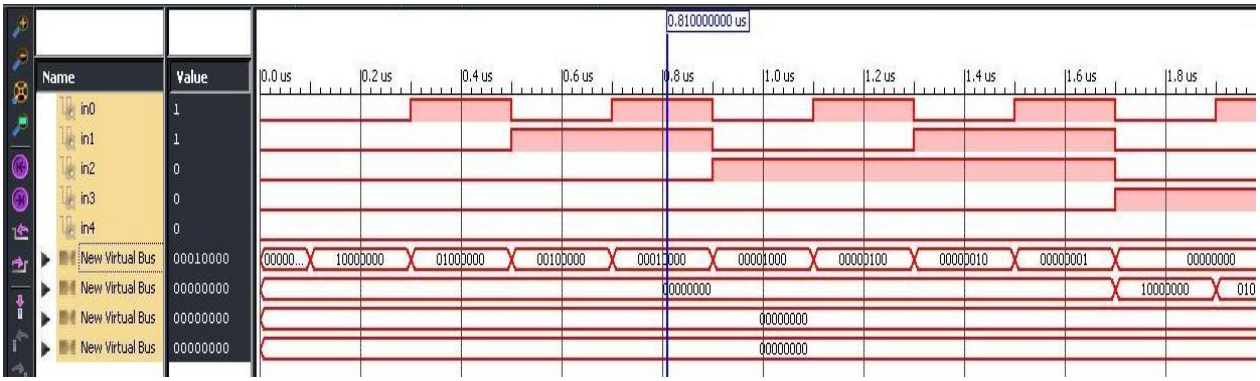

Figure 14: 5:32 DECODER RESULT (A)

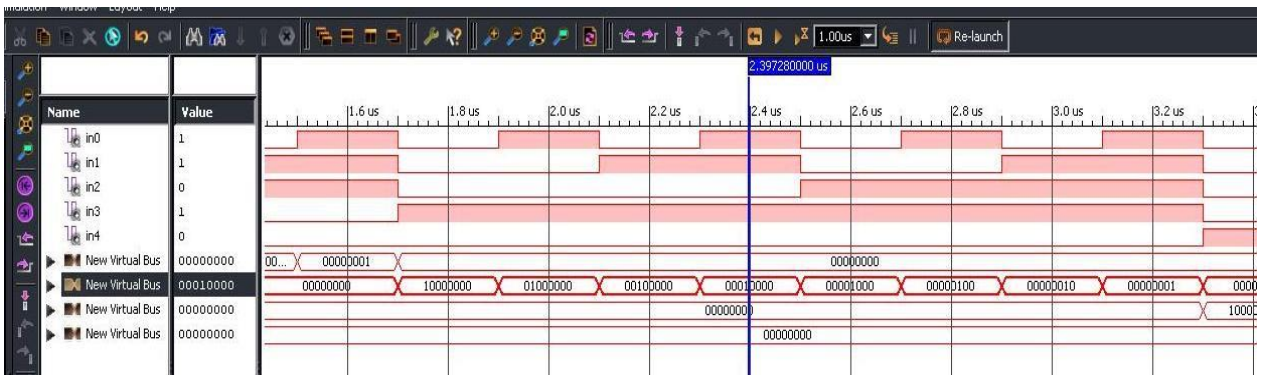

Figure 15: 5:32 DECODER RESULT (B)

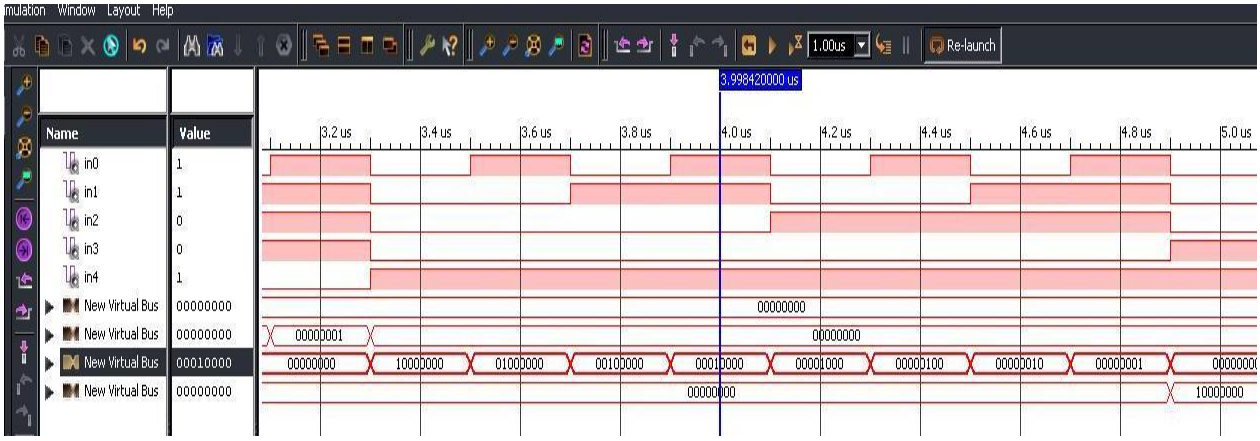

Figure 16: 5:32 DECODER RESULT (C)

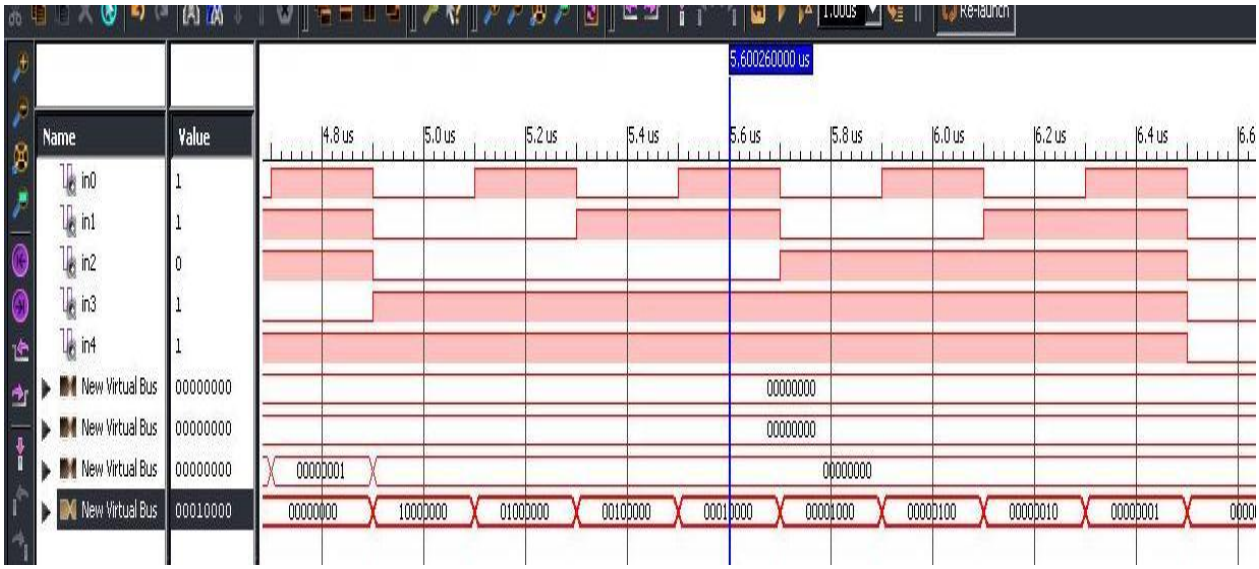

Figure 17: 5:32 DECODER RESULT (D)

8:1 MUX Feynman gate is used to copy the select bits SEL0 and SEL1, by giving B input '0'. Inputs v_in1 to v_in4 are connected to 4:1 mux1 and Inputs v_in5 to v_in8 are connected to 4:1 mux2. Using selection bits SEL0 and SEL1, corresponding input is selected. Mux output from these 4:1 mux are connected to a 2:1 mux whose selection bit is SEL2.. To visualise the results, Inputs v_in1, v_in3, v_in5 and v_in7 are given '0' and v_in2, v_in4, v_in6 and v_in8 are given '1'. By giving combination of Selection bits with different timing, the output of mux is proved. In the figure16., at 500ns, sel0 is '0', sel1 is '1' and sel2 '0' corresponding to v_in3 (low), connected to muxoutput. Muxoutput has be linked to the timing of select bit timings, to verify the results.

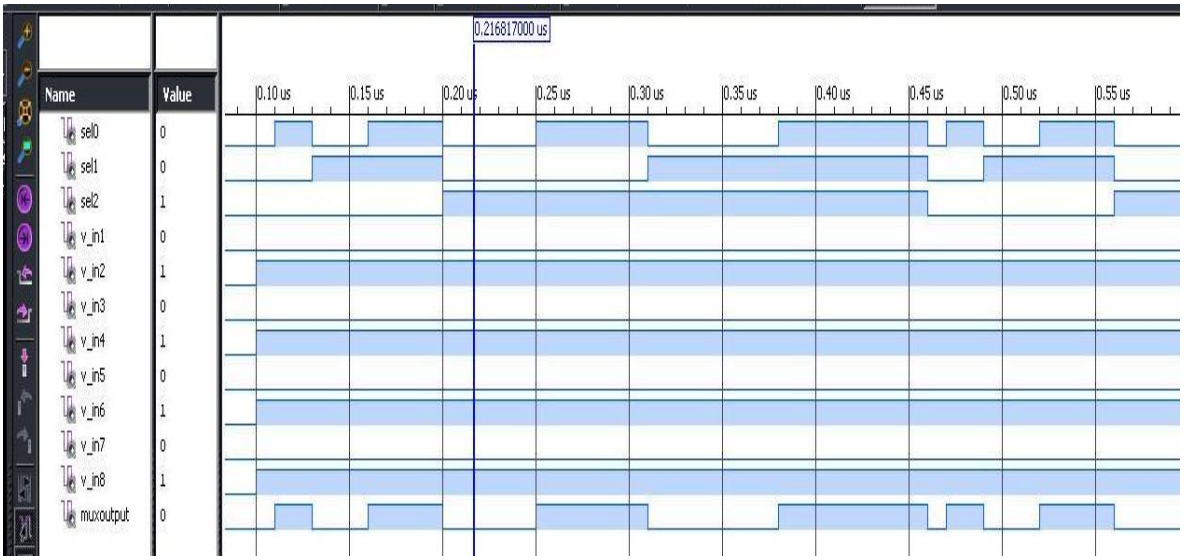

Figure 18: 8:1 MULTIPLEXER RESULT

16 BIT LATCH A short pulse is given as reset. 20ns clock is there at the input (clkin). Inputs D0 to D15 are given with '1' (11111111 11111111) at 0.280us. It is the falling edge of the input clock (clkin) and the DOUT becomes 11111111 11111111 on the risining edge of the input clock, at 0.290us. Similarly different16bit inputs 01010101 01010101, 10101010 10101010, 1111111111 00000000 and 00000000 1111111111 are given at datain and the DOUT is checked. It is observed that the DOUT matches the datain and results are verified.

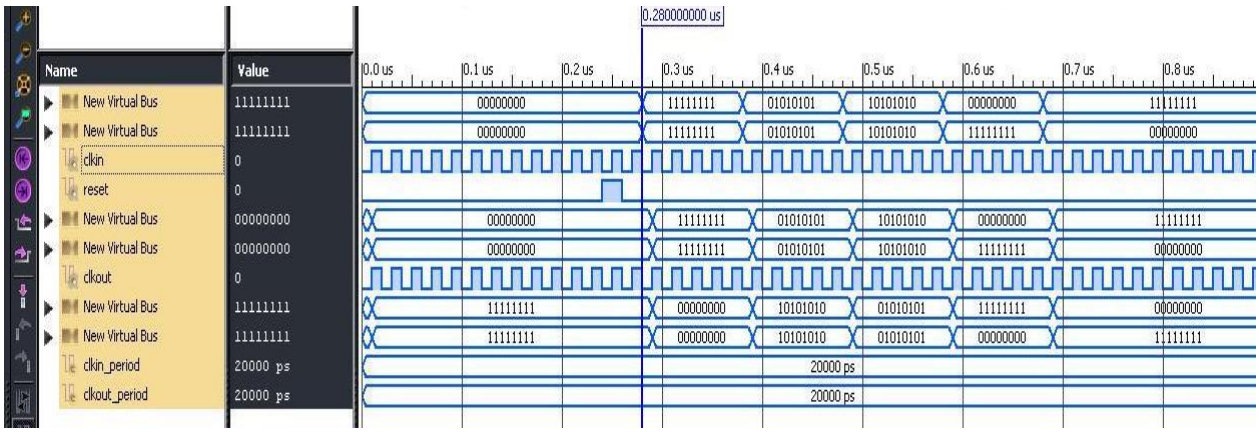

Figure 19: 16 BIT LATCH RESULT

The circuit has been simulated and functionality is verified using Xilinx. The circuit under study is designed [8] in Xilinx using VHDL code, simulated and verified. It is built on Tanner Tool. Garbage output of the designed circuits with existing design are compared. These circuits are simulated on Field Programmable Gate Arrays (FPGAs) using VHDL code and simulated on Isim. Reduced Garbage outputs are achieved. In future more complex circuits can be designed using these simple sequential and combinational circuits. Circuits like Dual port RAM, memory arrays shall be built using decoders and Latch circuits. Reversible counter, comparator circuits can be improved in garbage output and constant input. Power reduction is more visible when the circuit is built on CMOS.

CIRCUIT	GARBAGE OUTPUTS		
	PREVIOUS METHOD	EXISTING METHOD	PROPOSED METHOD
D FLIPFLOP	NOT AVAILABLE	8	4
2 to 4 decoder[3]	3	2	0
3 to 8 decoder[4]	4	3	1
4 to 16 decoder	5	4	3
5 to 32 decoder	NOT AVAILABLE	NOT AVAILABLE	7
4×1 multiplexer	17	16	7
8×1 multiplexer	NOT AVAILABLE	NOT AVAILABLE	16
16bit latch	NOT AVAILABLE	NOT AVAILABLE	16

Table 1. COMPARISON OF GARBAGE OUTPUT

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